REMARKS/ARGUMENTS

Favorable consideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-3 and 5-22 are presently pending in this application, Claims 1, 10-12 and 19 amended by the present amendment.

In the outstanding Office Action, Claims 11-19 were objected to for informalities; Claims 1-3 and 5-22 were rejected under 35 U.S.C. §103(a) as being unpatentable over Azuma (U.S. Patent 6,836,011) in view of Turlik et al. (U.S. Patent 5,325,265), Farooq et al. (U.S. Patent 6,335,210), Ikeda (JP 11-054884), Milkovich et al. (U.S. 6,516,513), and JP 59-000996 (hereinafter "JP '996"); Claims 11-19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Azuma, Turlik et al., Farooq et al., Ikeda, Milkovich et al. and JP '996, and further in view of U.S. 6,452,807 to Berrett and U.S. 6,193,524 to Chang; Claims 2, 5, 9, 12, 14 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Azuma, Turlik et al., Farooq et al., Ikeda, Milkovich et al. and JP '996, and further in view of Uchikawa et al.; and Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Azuma, Turlik et al., Farooq et al., Ikeda, Milkovich et al. and JP '996, and further in view of U.S. 4,819,131 to Watari.

With regard to the claim objections, Claims 11 and 12 have been amended to correct the informalities noted in the Office Action. Therefore the objections have been overcome.

Turning now to the merits, Applicants' invention is directed to an interposer that can be provided between a package substrate and an IC chip electrically connected to the package substrate. As discussed in the background section of Applicants' specification, high frequency IC chips are typically made of a brittle porous material that is prone to cracking

under thermal stress. Thus, stress defects in the IC chip occur during loading of the substrate with the IC.[1] Applicants' invention is directed to addressing this problem.

Specifically, Applicants' amended Claim 1 recites an interposer configured to be located between a package substrate made of resin and an IC chip. The interposer includes an insulating base material, wherein a Young's modulus of the insulation base material is 55 to 440GPa and a thickness of the insulation base material is 0.05 to 1.5 times the thickness of the package substrate. Also recited is a plurality of through holes provided through the insulating base material, each of the plurality of through holes having a diameter of 125 μm or less and having formed therein a through hole conductor for connecting the package substrate with the IC chip, wherein the plurality of through holes in the insulating base material are arranged in the form of a grid. New Claim 11 also recites these features with respect to a staggard arrangement of the through holes.

Thus, Applicants' amended Claims 1 and 11 recite,

> ***each of the plurality of through holes having a diameter of 125 μm or less*** and having formed therein a through hole conductor for connecting said package substrate with the IC chip, ***wherein the plurality of through holes in the insulating base material are arranged in the form of a grid*** [(claim 1), ***staggered arrangement*** (claim 11)]."

As discussed in Applicants' specification, when the diameter of the through hole is 125 μm or less, the amount of heat generation increases in the through holes because conductor resistance increases. In particular, the through hole connecting to a power source or a ground terminal of an IC chip generates high heat. The present invention is directed to this situation in which a small diameter through hole (125 μm or less) generates excessive heat, and the claimed invention addresses this issue by arranging the plurality of through holes in the insulating base material "in the form of a grid (claim 1) or a staggered arrangement (claim 11)."

[1] US Patent Publication No. 2006/0202322 (Applicants specification) at paragraph 4.

Specifically, as discussed in Applicants' specification,

> If the diameter of the through hole is 125 μm or less, it is effective that the through holes connected to the power source terminal and ground terminal of the IC are disposed in the form of a grid or in the staggered fashion. The reason is that the amount of heat generation increases in the through holes connected to the power source and ground terminal of the IC because conductor resistance increases. If the through holes are disposed in the form of a grid or in the staggered fashion, they are disposed uniformly. Thus, the temperature distribution of the interposer at the time of usage becomes uniform so that no stress concentrates on any specific location thereby the insulation layer of the IC chip being not damaged. Further, the physical property (thermal expansion coefficient, Young's modulus and the like) of the insulation base material just below the IC chip becomes uniform because the through holes are formed uniformly.[2]

In contrast to the invention of Claims 1 and 11, none of the cited references disclose the feature of the plurality of through holes having a diameter of 125 μm or less. In fact, Applicants cannot find any discussion in the cited references of through hole diameter with respect to electrical resistance and heat generation. Thus, none of the cited references disclose the "diameter of 125 μm or less" feature, which can cause the reliability problem discussed in the specification, or the additional feature of the through holes being in a grid or staggered arrangement, which can mitigate any such reliability problem. In this regard, Applicants note that the outstanding Office Action is silent about the limitation of a diameter of 125 μm or less, which was previously included in dependent Claims 10 and 19. Therefore, amended independent Claims 1 and 11 patentably define over the cited references.

Applicants' Claims 1 and 10 also recite that a "Young's modulus of insulation base material is 55 to 440Gpa and a thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate." As discussed in the Amendment filed August 1, 2007, none of the cited references disclose this feature, or indeed anything about thickness

[2] Applicants' specification at paragraph 23.

values of the interposer in relation to the package substrate. Nor do the cited references disclose scaled drawings by which one could measure and calculate the thickness range based solely on the drawings. The newly cited references to Berrett and Chang are not cited for these features and cannot correct the deficiencies of the primary references as noted in the August 1st amendment.

As also noted in the August 1st amendment, there is no reason to combine the claimed interposer thickness range with the claimed Young's modulus range; it is the present inventors who analyzed thermal stress during loading of the IC onto the substrate under various conditions and discovered that the combined features of the claimed Young's modulus and the claimed thickness range provide an improved configuration that suppresses deformation of the insulation base material and crevice or breaking in the resin layer of the IC. The cited references do not disclose any importance of the thickness relationship of an interposer to a package substrate, let alone this relationship in combination with the claimed thickness range. In view of this, Applicants submit that the Office Action's combination of these features is impermissible hindsight reasoning based on Applicants' disclosure.

For the reasons discussed above, independent Claims 1 and 11 patentably define over the cited references. Further, as the remaining pending claims depend from Claims 1 or 11, these claims also patentably define over the cited references. Nevertheless, Applicants have amended dependent Claims 10 and 19 to further distinguish the claimed invention from the cited prior art. Amended Claims 10 and 19 recite that a diameter of the through hole is from 30 μm to 125 μm. As discussed in Applicants' specification, the 30 μm lower limit was discovered by the inventors when considering the strength of the conductive material within the through hole.[3] As noted above, the cited prior art references do not discuss the diameter

[3] Applicants' specification at paragraph 23.

of the through hole. Thus, amended Claims 10 and 19 provide addition bases for patentability over the cited references.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application and the present application is believed to be in condition for allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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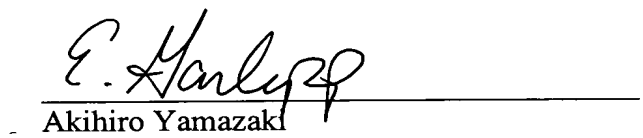

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